

REMARKS

This paper is in response to the official action of May 18, 2006, wherein claims 1-3 and 5-9 were rejected; reconsideration is requested.

The applicants have carefully reviewed and considered the official action and the references relied upon by the examiner. Entry of the above amendments is respectfully requested. Claims 1 and 5-8 have been amended to more clearly define the invention, without adding new matter.

Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,380,029) and Dong et al. (US 2002/0068398).

Independent claim 1 recites the steps of performing an annealing process to crystallize the tungsten silicide film and performing a first etching process to etch the crystallized tungsten silicide film and the second polysilicon film under the tungsten silicide film at one time using the same etching gas after a prior annealing process.

The etch rate of the crystallized tungsten silicide film (22b) is similar to that of the second polysilicon film (20) for the control gate electrode due to the annealing process. As a result, the tungsten silicide film (22b) and the second polysilicon film (20) for the control gate electrode can be etched at one time using the same etching gas.

Also, the etching process to etch the tungsten silicide film 22b and the second polysilicon film 20 for the control gate electrode is performed after the annealing process.

Therefore, the present invention can prevent any formation of recesses of the second polysilicon film.

However, referring to Chang, a number of etching processes are performed to define one or more stack structure(s). For example, capping layer 54 is first etched. Next, a tungsten silicide layer 50 and a poly-cap layer 52 on the tungsten silicide are etched at one time. Then, a polysilicon layer 48 for the control gate is etched.

That is, the tungsten silicide layer 50 and the polysilicon layer 48 are etched by distinct etching processes. Therefore, it is obvious that different etching gas is used for etching of the tungsten silicide layer 50 and the polysilicon layer 48.

Also, the etching process to etch the tungsten silicide layer 50 is performed after depositing the capping layer 54.

Accordingly, the applicants believe that claims 1-3, 5 and 8 are clearly different from what is disclosed in Chang and other cited references.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Dong as applied to claim 1 above, and further in view of Xu et al. (US 6,544,896).

Claims 6 and 7 depend from independent claim 1. Accordingly, applicant believes that the claims 6 and 7 are also in condition for allowance, since the claim 1 is in condition for allowance.

Therefore, the examiner is respectfully requested to pass this application to issue.

Should the examiner wish to discuss the foregoing or any matter of form in an effort to advance this application toward allowance, he is urged to telephone the undersigned at the indicated number.

Respectfully submitted,

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